WHAT IS CLAIMED IS:

1. A noise reduced printed circuit board comprising:

a substrate having at least two insulated layers for mounting conductive material;

a first set of conductive footprints being mounted on one of the insulated layers, each footprint of said first set being accessible from outside of the substrate and electrically connectable with a conductor extending from an electrical device, said first set of footprints being paired as the conductors in the electrical device while at least two unpaired conductors, the first and second conductor, are closely spaced from and cross talked with each other; and

a second set of conductive footprints each being located on an area of another insulated layers aligned with and spaced from one footprint of the first set and connected to another footprint of the first set; wherein

said one footprint of the first set is connected with the first conductor, and said another footprint of the first set is connected with a third conductor which is of the same pair as the second conductor.

2. The printed circuit board as recited in claim 1, wherein at least two conductive footprints of the second set are located on different insulated layers.

3. The printed circuit board as recited in claim 2, wherein footprints of the second set located on the nearer insulated layer to the layer where the first set of footprints is located have the same size as their corresponding aligned footprints of the first set, while footprints of the second set located on the farther insulated layer from the layer where the first set of footprints is located have an enlarged size larger than their corresponding aligned footprints of the first set.

4. The printed circuit board as recited in claim 3, wherein footprints of the first set are totally vertically aligned with their corresponding aligned footprints of the second set.

5. The printed circuit board as recited in claim 1, wherein each footprint of the second set has the same size as its corresponding aligned footprint of the first set.

6. The printed circuit board as recited in claim 5, wherein each footprint of the second set is totally vertically aligned with its corresponding aligned footprint of the first set.

7. The printed circuit board as recited in claim 1, wherein each footprint of the second set has an expanding size larger than its corresponding aligned footprint of the first set.

8. The printed circuit board as recited in claim 1, wherein every two footprints of the second set are connected to the same pair of footprints of the first set.

9. The printed circuit board as recited in claim 1, wherein each footprint of the first set is a solderably conductive pad.

10. The printed circuit board as recited in claim 1, wherein the printed circuit board is a built-in circuit board of a connector and all the necessary electronic components of the connector including conditioning component and terminal module are soldered on the printed circuit board.

11. A layout of a printed circuit board for noise reduction comprising:

a plurality of footprints being mounting on an outer face of a substrate of the printed circuit board, every two of said footprints being a signal-based pair when every footprints are electrically connected with a corresponding conductor from an electrical device;

a plurality of connecting conductive traces each being electrically connected to one footprint, portions of every trace extending along at least one intermediate layer located in the substrate of the printed circuit board for easiness to be electrically connected to other functional circuit of the printed circuit board; wherein

each trace connected to a first chosen pair of footprints is relocated to have portion of them pass through an area of the intermediate layer vertically spaced from the location of one footprint of a second chosen pair on the outer face of the substrate and an expanded conductive footprint is formed over there to couple with the footprint it faces.

12. The layout of the printed circuit board as recited in claim 11, wherein the expanded conductive footprint connected to one footprint of the first chosen pair is coupled with the footprint of the second chosen pair which bears a coupled signal from the electrical device when the conductor connected to said footprint of the second chosen pair is coupled with the conductor connected to the other footprint of the first chosen pair before the signals are transferred to the corresponding footprints.

13. The layout of the printed circuit board as recited in claim 11, wherein at least one expanding conductive footprints has the same size as its coupling footprint mounted on the outer face.

14. The layout of the printed circuit board as recited in claim 11, wherein at least one expanding conductive footprints has a size larger than its coupling footprint mounted on the outer face.

15. The layout of the printed circuit board as recited in claim 11, wherein the substrate has at least two different intermediate layers and at least one conductive trace portion extends along every intermediate layer.

16. The layout of the printed circuit board as recited in claim 15, wherein the expanding conductive footprints located at one intermediate layer far from the outer face has a size larger than its coupling footprint mounted on the outer face, and the expanding conductive footprints located at the other intermediate layer near the outer face has the same size as its coupling footprint mounted on the outer face.

17. A connector assembly having at least two mating ports to be engaged with a mating connector respectively, comprising:

a substrate having an electrical circuit layout on at least two insulated layers;

electronic components being electrically mounted on the substrate, at least one electronic component being used for each of the mating ports and having at least first and second pairs of conductors inside, one conductors of the first pair being closely parallel to and cross talked with one conductor of the second pair; wherein

said layout has two sets of footprints used to connect with the paired conductors from the electronic components of each mating port, and said two sets of footprints are located on a different insulated layer of the substrate respectively,

the footprint connected with said one conductor of said first pair of the electronic component couples with one footprint of a third set which is electrically connected to the footprint where the other conductor of said second pair not cross talked with said one conductor of said first pair is connected.

18. A printed circuit board comprising:

a substrate having at least two insulated layers;

a plurality of footprints being mounting on one insulated layer of the substrate of the printed circuit board, every two of said footprints being a signal-based pair when every footprints are electrically connected with a corresponding conductor from an electrical device;

a plurality of connecting conductive traces each being electrically connected to one footprint, the traces connected respectively to every footprint of one chosen pair being located on two different insulated layers; wherein

said traces located on two different insulated layers are aligned with each other along a predetermined distance.

19. A printed circuit board having conductive traces arrangement for reducing cross-talk therebetween, including

a substrate defining at least three mounting surfaces;

a first conductive trace including first, second and third sections;

a second conductive trace including first, second and third sections;

a third conductive trace including first, second and third sections; and

wherein the first section of the first, second and third conductive traces are all arranged in a common mounting surface;

wherein the second section of the first conductive trace is arranged in a second mounting surface and in align with the first section of the second

conductive trace;

wherein the third section of the first conductive trace is align with the third section of the third conductive trace.

20. A printed circuit board comprising:

first, second and third layers stacked one another;

first, second, third and fourth traces side by side located on the first layer in sequence, said first trace and said fourth trace being a differential pair, and said second trace and said third trace being another differential pair;

a fifth trace located on the second layer, vertically aligned with the first trace and electrically connected to the third trace for somewhat counterbalancing crosstalk between the first trace and the second trace generated around the first layer; and

a sixth trace located on the third layer, vertically aligned with the fourth trace and electrically connected to the second trace for somewhat counterbalancing crosstalk between the third trace and the fourth trace generated around the first layer; wherein

a distance between the first layer and the second layer is different from that between the first layer and the third layer, and a size of said fifth trace and that of the said sixth trace are dimensioned according to those distances.